St. Joseph's Institute of Technology

St. Joseph's Group of Institutions

OMR, Chennai – 119

Department of Electronics and Communication Engineering
(Accredited by NBA)

FACULTY DETAILS

Staff Name:	Dr. N.ABDUR RAHMAN
Designation:	Assistant Professor
Date of Birth:	01/07/1986
Educational Qualification:	M.Tech., Ph.D
Area of Interest:	VLSI , Embedded System and IoT, Wireless Communication
Years of Experience:	14 Years and 1 Months
Area of Research:	Certain Investigations On Low Power By-Passing 2d Multipliers Design Using Different Types Of Full Adder Logics
No. of Students Project Guided	32 UG projects and 4 PG Projects
Supervisor	--
FDP & Workshop Funding	Nil
Research Projects (Granted)	Nil
R & D Activities	Nil
Consultancy	Nil

Publications Details:	**Journal Publications:** • Dr. Abdur Rahman, September 2024, paper titled "Energy-Efficient Optimal Sink Placement Using Extended Pelican Optimization-Based Clustering with Voronoi Node-Based Displacement" has been published in International journal of Communication System in Wiley Publications, , Volume:38, Issue no. 3, listed in Anna University's Annexure 1. Impact Factor:1.70. Online ISSN No.1099-1131 (Sci Direct) • Anandan R, Abdur Rahman, December 2024, paper titled "CCOA-AdalLS: Hybrid Beamforming Using Chaotic Chebyshev Aquila Optimization for mmWave Massive MIMO" has been published in International journal of Communication System in Wiley Publications, , Volume:38, Issue no. 2, listed in Anna University's Annexure 1. Impact Factor:1.70. Online ISSN No.1099-1131 (Sci Direct) • Suresh Kumar, N & Paramasivam, K 2019, 'Energy efficient low-power full-adder by 65 nm CMOS technology in ALU', Concurrency and Computation-Practice & Experience, vol.31, no.12, pp. 1-6. Impact Factor: 1.167. Online ISSN No.1532-0634 (Sci Direct) • Paramasivam K., Suresh Kumar N. (2019). Design and Analysis Of Low Power Full Adder Using 65nm CMOS Technology. International Journal of Recent Technology and Engineering, 7(4),124-128. (SCOPUS) • Paramasivam K., Suresh Kumar N. (2019). Minimum Power Consumption High Efficiency Bypassing-Based 2d Multiplier Design Using 65nm CMOS Technology. International Journal Of Recent Technology And Engineering, 7(4),119-123. (SCOPUS) • Paper published entitled "A Novel Design for Power Reduction in Arithmetic Circuits Using MTCMOS Technology" for the Journal of VLSI Design Tools & Technology, ISSN:2249-474X, Volume 4 Issue 1, 2014, 1-7p. • Sureshkumar N, K.Paramasivam, "Bypassing-Based multiplier Design: A Tutorial and Research Survey" Journal of Applied Engineering Research, ISSN 0973-4562 Vol. 10 No29(2015),22606-22613p. • Abdur Rahman N, Sumathi.K, Gunavathi.A (2021). Intelligent Remainder Medicine Pill Box using IOT. International Journal of Infokara Research an UGC care approved journal, Volume 10, Issue 5 May 2021. (UGC Approved Journal) **Conference:** • Presented a paper entitled "Machine Leaning Enhanced Survillance for Proactive Highway Accident Detection" for the International conference "ARAM'24" held at SSN College of Engineering, Chennai, during Mar 28th to 29th ,2024

	• Presented a paper entitled "Intelligent Remainder Medicine Pill Box using IOT" for the International conference "ICCSE'21" held at Indra Ganesan College of Enginnering, Trichy, during Apr 09th to 10th ,2021 • Presented a paper entitled "Less power consumption high efficiency Bypassing-based Multiplier design using 65nm CMOS Technology" for the International conference "I-STEM 2018" held at Kumaraguru college of Technology, Coimabatore, during May 10th to 12th ,2018. • Presented a paper entitled "Low power Bypassing-based Multiplier design using adiabatic logic" for the International conference "ICETE 2011" held at NMAM Institute of Technology, Nitte, Karnataka, during May 4th & 5th ,2011. • Presented a paper entitled "Low power 2-Dimensional Bypassing-based Multiplier design using Positive Feedback adiabatic logic" for the International conference "ICMEET-2K11" at MAGNA Engineering College, Chennai, held on 12 Apr 2011. • Presented a paper entitled "Implementation of Low Power VlSI Design for Digital Systems" for the National conference on Information & Communication Systems "ICS-2012" at Info Institute of Engineering College, Coimbatore, held on 8th 9th March 2012.
FDP & Workshop Attended Details:	• Attended Five Days Online Faculty Development Program on "Teaching, Leaning and Research Methodology" held from 19th Feb to 23th Feb 2024 Organized by Artificial Intelligence and Data Science, St. Xavier catholic College of Engineering (Autonomous), Nagercoil. • Attended Seven Days Online Faculty Development Program on "Personality Development for Teachers HEI's" held from 28th June to 04th July 2023 Organized by MSME Registered IOT Academy, Coimbatore. • Attended One week Online Faculty Development Program on "Nano-materials & Nan mechanics and their application in devices and sensors" held from 28th June to 07th July 2021 Sponsored by AICTE Training And Learning (ATAL) Academy at Indian Institute of Technology (IIT) Hyderabad. • Attended One week Online Faculty Development Program on " Electret Applications in Sensors, Microelectronics and Actuators" held from 05th July to 09th July 2021 Sponsored by AICTE Training And Learning (ATAL) Academy at Shri.G.S.I.T.S, Indore. • Attended One day Online Workshop on "How to Conduct the Student Induction (SIP) Program" held from 20th Sept 2021 Organized by All India Council for Technical Education (AICTE). • Attended One week Faculty Development Program on

	"Electronic System Design" held from 26th May to 01st June 2014 Sponsored by TEQIP-II at Government College of Engineering, Bargur-635104. • Attended Two weeks ISTE Workshop on "Signals and System" during 02nd to 12th Jan 2014 Conducted by Indian Institute of Technology (IIT), Kharagpur at Sri Shanmugha College of Engineering and Technology, Salem. • Attended three days Faculty Development Program on "Mission 10X – Engineering Faculty Workshop" organized by WIPRO on 18th to 20th Dec 2013. • Attended two days Faculty Development Program on "Analog System Design Using Texas Instruments Analog System Lab Kit (ASLK)" organized by the Department of E.C.E at Anna University Coimbatore on 5th & 6th July 2012 in association with Texas Instruments, Bangalore. • Attended One day Workshop on "Embedded Memory Design for System on Chip" during 14th December 2013 conducted by department of E.C.E. at PSG College of Technology, Coimbatore-641 004 • Participated in International Workshop on "Research and Journal Publication" held at Christ the King Engineering College, Coimbatore, on 18.01.2012. • Attended two days National workshop on "Engineering Perspectives for Diabetes and Epilepsy Health care" during 28th & 29th February 2012 at Bannari Amman Institute of Technology, Sathyamangalam conducted by department of E.C.E. • Attended two days Faculty Development Program on "Recent Trends in VLSI Computation" during 21th & 22th March 2016 conducted by department of E.C.E. at Sri Ramakrishna Engineering College, Coimbatore-641 022
Professional Membership:	LIFE MEMBER OF **ISTE – LM81638**